IN THE CLAIMS

1. (Previously Presented) A method for communicating data, comprising:

communicating a first set of data from a first channel to a first serial-to-parallel converter and communicating a second set of data from a second channel to a second serial-to-parallel converter;

converting the first and second sets of data to a parallel format;

monitoring the first and second serial-to-parallel converters in order to determine when one or more words of the respective data sets have accumulated in each of the first and second serial-to-parallel converters;

writing one or more of the words that have accumulated in each of the first and second serial-to-parallel converters to a selected one of first and second memory banks;

monitoring, by a single scheduler, the first and second memory banks to determine when enough of the words that were written to each of the first and second memory banks have formed one or more cells; and

reading one or more of the cells out of a selected one of the first and second memory banks such that they may be communicated to an output communications link.

2. (Original) The method of Claim 1, further comprising generating a memory address for each of the one or more words to be written into the first and second memory banks, the memory addresses designating the space where the one or more words are written to in the first and second memory banks.

3. (Original) The method of Claim 2, further comprising receiving one or more of the cells that are read out of the first and second memory banks at an ATM switch.

4. (Original) The method of Claim 1, wherein the reading of the cells out of the first and second memory banks is executed by a scheduler that is coupled to the first and second memory banks and a Utopia bus.

5. (Original) The method of Claim 1, further comprising providing a select controller, which is coupled to the first and second serial-to-parallel converters, the select controller being operable to determine which of the first and second memory banks the words, which have accumulated in each of the first and second serial-to-parallel converters, are written to.

6. (Original) The method of Claim 5, further comprising communicating a write enable signal from the select controller to a selected one of the first and second memory banks to indicate that one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, is ready to be written.

7. (Original) The method of Claim 6, further comprising signaling, by the select controller, to a multiplexer to communicate one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, to a selected one of the first and second memory banks.

8. (Original) The method of Claim 1, further comprising incrementing an address associated with a selected one of the first and second memory banks each time one of the words, which have accumulated in each of the first and second serial-to-parallel converters, is written to one of the first and second memory banks.

9. (Previously Presented) An apparatus for communicating data, comprising:

a multiplexer operable to receive one or more words associated with a respective one of a first and a second set of packet data, wherein the first and second sets of packet data are associated with a first channel and a second channel respectively;

first and second memory banks each coupled to the multiplexer and each operable to receive one or more of the words from the multiplexer; and

a scheduler coupled to each of the first and second memory banks and operable to monitor the first and second memory banks in order to determine whether the first and second memory banks have accumulated enough words to form a cell, the scheduler operable to read one or more cells out of a selected one of the first and second memory banks, wherein each of the cells comprises a plurality of the words from a respective one of the first and second sets of packet data.

10. (Original) The apparatus of Claim 9, further comprising a first write controller associated with the first channel and a second write controller associated with a second channel, wherein the first and second write controllers are each operable to communicate one or more of the words to the multiplexer.

11. (Original) The apparatus of Claim 10, further comprising a select controller coupled to the multiplexer and operable to determine which of the first and second memory banks the words are written to.

12. (Previously Presented) The apparatus of Claim 11, further comprising first and second serial-to-parallel converters, the first serial-to-parallel converter coupled to the first write controller and operable to convert the first set of packet data to a parallel form before the first set of packet data is received by the first write controller, the second serial-to-parallel converter coupled to the second write controller and operable to convert the second set of packet data to a parallel form before the second set of packet data is received by the second write controller.

13. (Previously Presented) The apparatus of Claim 9, further comprising a Utopia bus coupled to the scheduler and operable to communicate one or more cells from the scheduler to an asynchronous transfer mode (ATM) switch.

14. (Original) The apparatus of Claim 13, further comprising a demultiplexer coupled to the ATM switch and the Utopia bus and operable to provide a communications interface therebetween.

15. (Original) The apparatus of Claim 9, further comprising a dual-port memory coupled to the multiplexer and the scheduler, wherein the first and second memory banks are included within the dual port memory.

16. (Previously Presented) A system for communicating data, comprising:

means for communicating a first set of data from a first channel to a first serial-to-parallel converter and communicating a second set of data from a second channel to a second serial-to-parallel converter;

means for converting the first and second sets of data to a parallel format;

means for monitoring the first and second serial-to-parallel converters in order to determine when one or more words of the respective data sets have accumulated in each of the first and second serial-to-parallel converters;

means for writing one or more of the words that have accumulated in each of the first and second serial-to-parallel converters to a selected one of first and second memory banks;

means for monitoring, by a single scheduler, the first and second memory banks to determine when enough words have accumulated in the first and second memory banks to form one or more cells; and

means for reading one or more of the cells out of the first and second memory banks such that they may be communicated to an output communications link.

17. (Original) The system of Claim 16, further comprising means for generating a memory address for each of the one or more words to be written into the first and second memory banks, the memory addresses designating the space where the one or more words are written to in the first and second memory banks.

18. (Original) The system of Claim 17, further comprising means for receiving one or more of the cells that are read out of the first and second memory banks at an ATM switch.

19. (Original) The system of Claim 18, wherein the reading of the cells out of the first and second memory banks is executed by a scheduler that is coupled to the first and second memory banks and a Utopia bus.

20. (Original) The system of Claim 16, further comprising means for determining which of the first and second memory banks the words, which have accumulated in each of the first and second serial-to-parallel converters, are written to.

21. (Original) The system of Claim 20, further comprising means for communicating a write enable signal to a selected one of the first and second memory banks to indicate that one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, is ready to be written.

22. (Original) The system of Claim 21, further comprising means for signaling to a multiplexer to communicate one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, to a selected one of the first and second memory banks.

23. (Original) The system of Claim 16, further comprising incrementing an address associated with a selected one of the first and second memory banks each time one of the words, which have accumulated in each of the first and second serial-to-parallel converters, is written to one of the first and second memory banks.

24. (Previously Presented) Software for communicating data embodied in a computer readable medium and operable to:

communicate a first set of data from a first channel to a first serial-to-parallel converter and communicating a second set of data from a second channel to a second serial-to-parallel converter;

convert the first and second sets of data to a parallel format;

monitor the first and second serial-to-parallel converters in order to determine when one or more words of the respective data sets have accumulated in each of the first and second serial-to-parallel converters;

write one or more of the words that have accumulated in each of the first and second serial-to-parallel converters to a selected one of first and second memory banks;

monitor, by a single scheduler, the first and second memory banks to determine when enough words have accumulated in the first and second memory banks to form one or more cells; and

read one or more of the cells out of the first and second memory banks such that they may be communicated to an output communications link.

25. (Original) The software of Claim 24, further operable to generate a memory address for each of the one or more words to be written into the first and second memory banks, the memory addresses designating the space where the one or more words are written to in the first and second memory banks.

26. (Original) The software of Claim 25, further operable to receive one or more of the cells that are read out of the first and second memory banks at an ATM switch.

27. (Original) The software of Claim 26, wherein the reading of the cells out of the first and second memory banks is executed by a scheduler that is coupled to the first and second memory banks and a Utopia bus.

28. (Original) The software of Claim 24, further operable to determine which of the first and second memory banks the words, which have accumulated in each of the first and second serial-to-parallel converters, are written to.

29. (Original) The software of Claim 24, further operable to communicate a write enable signal to a selected one of the first and second memory banks to indicate that one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, is ready to be written.

30. (Original) The software of Claim 24, further operable to signal to a multiplexer to communicate one or more of the words, which have accumulated in each of the first and second serial-to-parallel converters, to a selected one of the first and second memory banks.

31. (Original) The software of Claim 24, further operable to increment an address associated with a selected one of the first and second memory banks each time one of the words, which have accumulated in each of the first and second serial-to-parallel converters, is written to one of the first and second memory banks.

32. (Previously Presented) An apparatus for communicating data, comprising:

a multiplexer operable to receive first and second sets of data, wherein the first and second sets of data are associated with a first channel and a second channel respectively;

a first write controller associated with the first channel and a second write controller associated with the second channel;

first and second serial-to-parallel converters, the first serial-to-parallel converter coupled to the first write controller and operable to convert the first set of data to a parallel form before the first set of data is received by the first write controller, the second serial-to-parallel converter coupled to the second write controller and operable to convert the second set of data to a parallel form before the second set of data is received by the second write controller;

first and second memory banks each coupled to the multiplexer and each operable to receive from the multiplexer one or more words that have accumulated in each of the serial-to-parallel converters and that comprise a portion of a selected one of the first and second sets of data;

a scheduler coupled to each of the first and second memory banks and operable to monitor the first and second memory banks in order to determine whether the first and second memory banks have accumulated enough words to form a cell, the scheduler operable to read a cell out of a selected one of the first and second memory banks, wherein the cell comprises a plurality of the words; and

a select controller coupled to the multiplexer and operable to determine which of the first and second memory banks the words are written to.